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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/888,663	06/25/2001	Michael H. Perrott	026-0012	8862

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EXAMINER	
GLENN, KIMBERLY E	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 06/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/888,663	PERROTT, MICHAEL H.	
	Examiner	Art Unit	
	Kimberly E Glenn	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2 and 5* is/are allowed.

6)☒ Claim(s) *1 3 4 6 15-20 23 31 33-39* is/are rejected.

7)☐ Claim(s) *8-12 14 21 22 24-30 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim R jections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1,3,4, 6, 7, 15-20, 23, 31, 35 and 36-39 are rejected under 35 U.S.C. 102(e) as being anticipated by Peragine US Patent 6,623,185.

Peragine disclose figure 4, a circuit comprising a clock and data recovery (CDR) circuit 404, receiving an input signal from an optical receiver a logic circuit 408, a window detector 406. The CDR circuit includes a phase detector, a loop filter and a voltage-controlled oscillator (VCO) to recover the degraded signal. Three designs of CDR circuit are commercially available-a Surface Acoustic Wave (SAW) filter configuration; a Voltage-Controlled Crystal Oscillator (VCXO) configuration that includes a PLL; or an all silicon VCO configuration. Figure 3 discloses three sample windows 302, 304 and 306. In window 304, when a true data signal is present, then no transitions are detected during that sampling window. In contrast, during sampling windows 302 and 306, frequent data transitions are detected, indicating that during these sampling windows 302 and 306, an LOS event occurred. These data transitions can advantageously be counted, and if the number of transitions in a sampling window

exceeds a predetermined threshold number, an LOS indication is generated. By counting the transitions or lack of transitions, the CDR, which includes a phase locked loop, is evaluated. Inherently, the Phase locked loop will adjust the frequency of the variable frequency oscillator circuit in response to the PLL not being locked to the input data stream. A phase locked loop is defined as an electronic circuit with a voltage or current driven oscillator that is constantly adjusted to match in phase (and thus lock on) the frequency on an input signal. The method steps to the above-disclosed apparatus are inherent. (See figures 3 and 4 and column 3; line 10 and column; 4 line 57)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13, 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peragine US Patent 6,623,185.

Peragine teaches figure 4, a circuit comprising a clock and data recovery (CDR) circuit 404, receiving an input signal from an optical receiver a logic circuit 408, a window detector 406. The CDR circuit includes a phase detector, a loop filter and a voltage-controlled oscillator (VCO) to recover the degraded signal. Three designs of CDR circuit are commercially available-a Surface Acoustic Wave (SAW) filter configuration; a Voltage-Controlled Crystal Oscillator (VCXO) configuration that includes

a PLL; or an all silicon VCO configuration. Figure 3 discloses three sample windows 302, 304 and 306. In window 304, when a true data signal is present, then no transitions are detected during that sampling window. In contrast, during sampling windows 302 and 306, frequent data transitions are detected, indicating that during these sampling windows 302 and 306, an LOS event occurred.

Thus Peragine is shown to teach all the limitations of the claim with the exception of the oscillator circuit being a ring oscillator or a tank circuit having an inductive element.

One of ordinary skill in the art would have found to obvious to replace the oscillator of Peragine with a ring oscillator or tank circuit since examiner takes notice that each of theses are conventional voltage controlled oscillators and have been made use of in clock data recovery art and the selection of any of these known conventional VCOs would be within the level of ordinary skill in the art.

Response to Arguments

Applicant's arguments filed 4/14/04 have been fully considered but they are not persuasive. Applicant argues that the Peragine reference does not teach or suggest the output of the oscillator is varied based on the LOS condition. Applicant's claims as amend do not recite the limitation regarding the loss of signal output being applied to the oscillator. Applicant amended the claim by adding the limitation that the output frequency of the variable frequency oscillator is adjusted in response to a determination that the phase locked loop has not locked to the timing of the input data stream. Inherently, a phase locked loop will adjust the frequency of the variable frequency

oscillator circuit in response to the PLL not being locked to the input data stream. A phase locked loop is defined as an electronic circuit with a voltage or current driven oscillator that is constantly adjusted to match in phase (and thus lock on) the frequency on an input signal.

Allowable Subject Matter

Claims 2 and 5 are allowed.

Claims 8-12,14,21,22,24-30 and 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: With regards to claim 2, the prior art of record does not disclose or fairly teach further evaluating over a plurality of time periods, each of the time periods including an increasing number of evaluation intervals, whether the PLL is locked to the timing of the input data stream according to a number of evaluation intervals having one or more transitions in the predetermined portion of the sample clock period. With regards to claim 5, the prior art of record does not disclose or fairly teach the evaluation intervals being at least as long as the minimum period of the frequency offset. With regards to claims 8-12, 14 and 21, the prior art of record does not disclose or fairly teach output frequency being adjusted by changing or the variable impedance associated with the oscillator circuit until lock is achieved. With regards to claim 22, the prior art of record does not disclose or fairly teach the output of the variable oscillator comprising of varying at least one of the control voltages and a control current supplied to the variable

oscillator. With regards to claims 24, 26 and 28, the prior art of record does not disclose or fairly teach the phase zone detect circuit includes a first data path and a second data path coupled to receive the input data stream, one of the first and second data paths being delayed with respect to the other, thereby defining the phase zone, and wherein an output signal supplied from the first and second data paths are coupled to a logic circuit to be logically compared. With regards to claims 39 30 and 32, the prior art of record does not disclose or fairly teach a variable impedance circuit forming part of the variable oscillator circuit; and wherein the control circuit is responsive to the indication that lock is not achieved, to vary the variable impedance circuit to thereby adjust the output of the variable oscillator circuit.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly E Glenn whose telephone number is (571)-272-1761. The examiner can normally be reached on Monday-Friday 7:30 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571)-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kimberly E Glenn
Examiner
Art Unit 2817

keg

Robert Pascal
Supervisory Patent Examiner
Technology Center 2800